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Improving IBIS-AMI Model Accuracy: Model-to-Model and Model-to-Lab Correlation Case Studies

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Abstract

As serial data link speed continues to increase and SerDes architecture becomes more complex, the IBIS Algorithmic Modeling Interface (IBIS-AMI) has become popular among system developers and SerDes vendors. To accurately and quickly predict high-speed link performance at a bit error rate (BER) of 1E-12 or lower, IBIS-AMI models need to accurately represent chip performance and be validated at certain levels. Two methods have been widely used to validate an IBIS-AMI model. The first method, model-to-model correlation, is used if the SerDes vendor already has an existing in-house models built on a certain computing platform (Matlab, C/C++, Python, etc.) and validated to be accurate. The second method, model-to-lab correlation, compares model simulation results to data acquired in lab testing. This paper presents case studies for both methods and compares favorable and unfavorable factors for both methods. 10G, 11.5G and 23G SerDes data are used as examples.

Author(s) Biography

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Yunong Gan is currently an IC Design Manager in the ING business unit at Broadcom Corp., Irvine, California. Since 2005, he has been working on SI and Modeling of high-speed SerDes for electrical and optical communication links. Previously, he was with Motorola and Corning and has developed transmitter and receivers for optical communication solutions. Yunong received his M.S. degree in Electrical Engineering from the University of Massachusetts at Amherst in 2000. He received his B.S. degree in Electronics Engineering from Tsinghua University, China in 1997.

Vivek Telang is a Senior Director of Engineering in the Physical Layer Products Group in Broadcom, where he has been working since 2004. His area of expertise is the system-level design and implementation of high-speed SerDes systems used in Broadcom 10G and 25G backplane and front-panel products. His current responsibilities include the design of 25G-100G SerDes systems. Vivek received his Bachelor's degree in Electrical Engineering from the Indian Institute of Technology in Bombay, India and his M.S. and Ph.D. from the University of Notre Dame. .

Magesh Valliappan is the manager of the SerDes architecture and design team at Broadcom. Since joining Broadcom in 2005, his work has focused on developing technology for delivering high-performance SerDes IP for electrical and optical applications. Mr. Valliappan received his M.S. degree from The University of Texas at Austin in Electrical and Computer Engineering and his B.S. degree from the Indian Institute of Technology, Madras in Electrical Engineering.

Fred S. Tang received his Ph.D. degree in Electrical Engineering from Stanford University in 1998. He joined Broadcom in 2008 and works on Coherent DSP algorithms, high-speed optoelectronic device simulation in ADS, Matlab, Rsoft, and VPI, optical link modeling and validation. From 2005 to 2008 he was with the Intel's Optical Platform Division, where he designed X2 and SFP+LRM transceivers. From 2001 to 2005 he was with Big Bear Networks where he made key contributions to the world's first serial 40G transponder, the X2-LRM module, and LRM stress generator. Prior to 2001, he worked in the areas of wavelength tunable VCSELs and photo detectors, pHEMTs, high-speed optoelectronic device modeling and optimization.

Todd Westerhoff is Vice President of software products for SiSoft. He has 34 years of simulation experience, including 17 years of signal integrity. Prior to SiSoft, Todd managed a signal integrity group that provided high-speed design services to various ASIC and system engineering groups within Cisco. Todd was also the SPECCTRAQuest Product Manager for Cadence Design Systems and a signal integrity consultant to a number of Fortune 500 companies. He has held product marketing positions at Compact Software, Racal-Redac, FutureNet, and HHB-Systems. Todd holds a Bachelors of Engineering degree in Electrical Engineering from the Stevens Institute of Technology in Hoboken, New Jersey.

Fangyi Rao received his Ph.D. in Theoretical Physics from Northwestern University in 1997. He joined Agilent EEsof in 2006 and works on analog/RF and SI simulation technologies in ADS and RFDE. From 2003 to 2006 he was with Cadence Design Systems where he made key contributions to the company's harmonic balance technology and perturbation analysis of nonlinear circuits. Prior to 2003, he worked in the areas of EM simulation, nonlinear device modeling, and optimization.

1. Introduction

With increasing data rates of SerDes channels and complexity of the associated digital equalization blocks, classic time-domain simulations with legacy IBIS and SPICE models have slowed to the point where their usefulness is limited. Extremely long simulation times associated with transistor level models and vendor-specific encryption increase the effort required to develop accurate models and decrease model portability. Furthermore, even when such models are developed, simulation throughput is limited and design validation takes a long time. With the release of the IBIS 5.0 in 2008 [1], Algorithmic Modeling Interface (AMI) [2] [3] has provided an Industry- standard way of simulating high-speed serial links with advanced signal processing elements, such as analog filters, FFE and DFE, etc. IBIS-AMI models offer orders-of-magnitude of improvement in simulation time, while IP remains hidden and protected within a compiled executable in binary format called from EDA tools through a standard interface. This standard interface allows AMI models to run on any EDA tools that support IBIS-AMI. With their high flexibility and good IP protection, AMI models have become the choice of many design customers and SerDes vendors.

To guarantee that an AMI model can correctly predict the performance of the corresponding chips, detailed procedures to validate accuracy of AMI models must be used by SerDes vendors. To date, there are two methods that have been widely used to validate IBIS-AMI models; model-to-model correlation and model-to-lab correlation. Model-to-model correlation utilizes existing in-house models developed by the SerDes vendors on certain platforms such as Matlab, C/C++, or Python, etc., where these models have already been validated and are known to be accurate. The Model-to-lab method compares simulation results with measured data acquired from Lab testing to ensure the developed IBIS-AMI model matches behavior observed with actual SerDes channels.

This paper is organized as follows. Section 2 describes the basics of SerDes designs. Section 3 introduces LinkEye® [4], Broadcom's in-house simulation tool. Section 4 describes model-to-model correlation for 11.5G SerDes; Section 5 presents model-to-lab correlation for the 10G and 23G SerDes designs. Section 6 discusses advantages and disadvantages of these two methods, and section 7 presents our conclusions.

2. Modeling of SerDes Channels Using IBIS-AMI

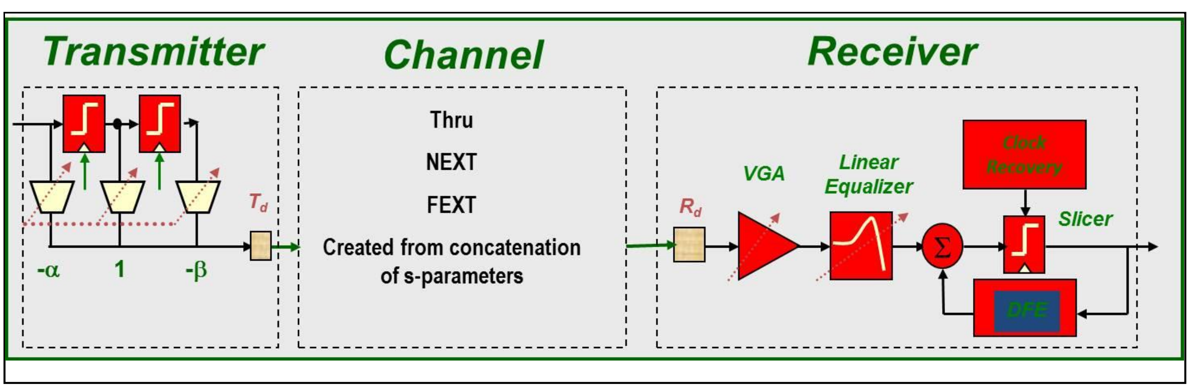


Figure 1. SerDes Block Diagram.

A typical SerDes interconnection model is shown in Figure 1. The transmitter (TX) consists of a Feed-Forward Equalizer (FFE) and TX driver. FFE in the TX uses pre-emphasis to "invert" the frequency roll-off in the channel. The receiver (RX) comprises a RX termination network followed by RX equalization (EQ), and clock / data recovery (CDR) circuits. Between the TX and RX, a channel model with the through path, near-end crosstalk (NEXT) and far-end crosstalk (FEXT), and package models is inserted. An IBIS-AMI model developed for such a SerDes channel can be divided into two parts. One is an analog portion describing the TX output driver, RX termination load, and TX/RX packages. The other part consists of algorithmic model that provide analog filtering and digital signal processing modeling equalization and CDR behavior in the TX and RX. Figure 2 shows a block diagram of an IBIS-AMI model.

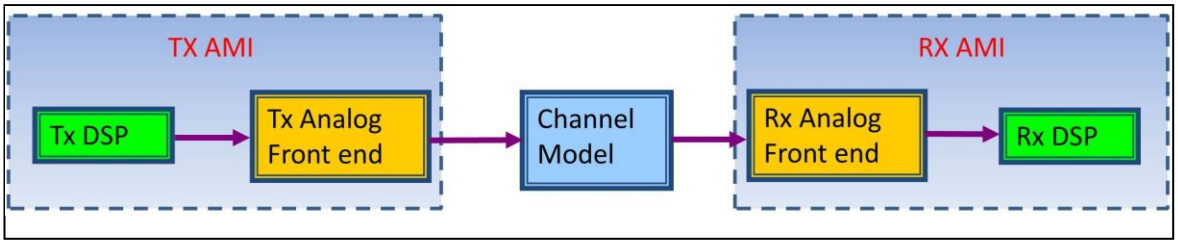


Figure 2. IBIS-AMI Model.

In Figure 2, TX DSP and RX DSP implement all the digital signal processing while all the other analog elements, such as TX driver, RX load, TX/RX packages and RX analog receive filtering, are included in the TX and RX analog front end, respectively.

3. LinkEye: A Broadcom In-House SerDes Modeling Tool

Broadcom's Infrastructure and Networking group has developed an in-house tool called LinkEye to simulate its SerDes products. LinkEye is a Matlab-based software tool used to estimate the performance of Broadcom SerDes using statistical analysis. LinkEye uses pulse response "Frequency-domain" analysis to predict BER, as shown in Figure 3, and can be configured to model different TX and RX modes corresponding to real chip settings. In LinkEye, the equalizer is optimized using minimum-mean-squared-error (MMSE) techniques, and the chip performance evaluation is based on detailed, worst-case error probabilities. LinkEye also considers on-chip impairments such as clock jitter and offset, front-end noise, and other detailed equalizer implementation penalties. Worst-case bit sequences are used to destructively add ISI and evaluate the impact of crosstalk. The composite noise Probability Density Function (PDF) is created by convolving PDFs of thermal noise, ISI, crosstalks, jitter, and other circuit non-idealities. The overall BER is calculated using detailed analytical techniques that combine the effects of all the impairments.

Throughout the years, LinkEye has been extensively correlated to real chip performance obtained through lab measurements. Correlation efforts involve identifying and measuring representative channels on backplanes or cables, simulating all channels including the effects of crosstalk, running lab bench tests with actual silicon, and correlating lab data with simulations. To take advantage of good correlation between LinkEye and lab test data, we only correlate our IBIS-AMI simulation results with the LinkEye simulations. This model-to-model correlation is faster and less expensive than lab measurement, and has the advantage that simulation results are more reproducible. In section 4, a case study in which a 11.5G IBIS-AMI model correlation to LinkEye model is presented.

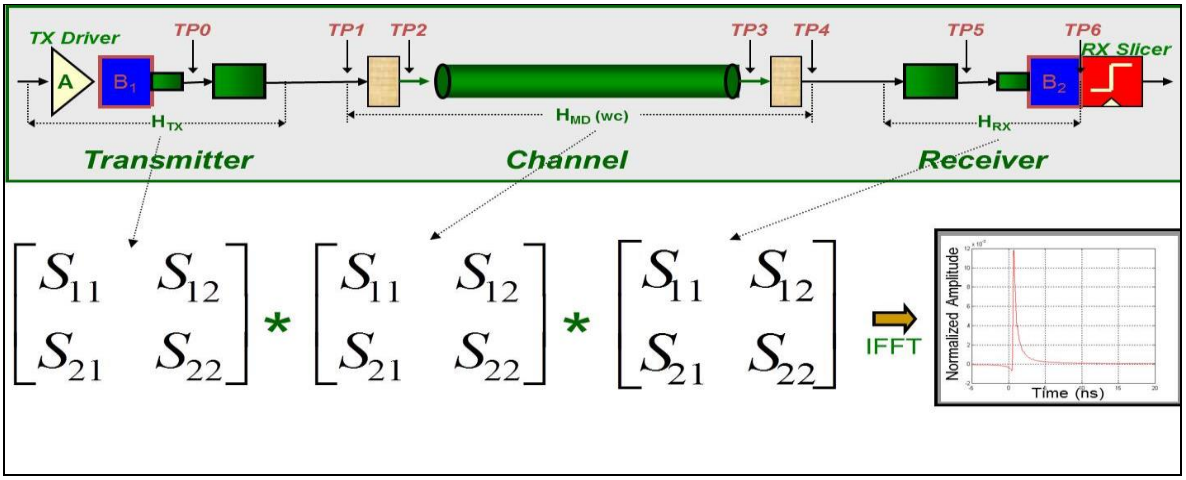


Figure 3. Linkeye Channel Simulation Model.

4. Case Study: IBIS-AMI Model Validation Through Model-to-Model Correlation

In this case study, we demonstrate how we split the entire correlation task into several stages and fine tune a 11.5G SerDes IBIS-AMI model to correlate with LinkEye. At the time we first built the 11.5G IBIS-AMI model, an on-die S-parameter to characterize the analog front end was just emerging as a flexible, accurate, and relatively simple new technique to replace the traditional IBIS element (analog buffer) model. We decided to use this technique on the 11.5G SerDes IBIS-AMI model and work closely with EDA vendors to understand the analytical background behind the on-die S-parameter method and fine tune our model.

After first version of the SerDes AMI model was built, we compared the optimized equalizer settings and the overall BER with the LinkEye simulation on some backplane channels as shown in Table 1. There are significant differences between AMI and LinkEye simulations indicating a poor correlation between the two models that needs to be fixed. The following sections show how we split the model into blocks and correlate them one by one.

Channel ID	AMI (Statistical Sim)				LinkEye			
	P.K.F	VGA	DFE1	BER	P.K.F	VGA	DFE1	BER
1	7	15	0.2601	3.00E-39	4	16	0.358	1.00E-69
2	7	15	0.2776	1.00E-39	5	16	0.354	1.00E-65
3	12	17	0.4727	2.00E-36	9	19	0.541	1.00E-45
4	15	22	0.7114	2.00E-28	15	22	0.741	1.00E-30
5	8	16	0.439	5.06E-09	5	17	0.475	1.00E-10
6	10	17	0.487	8.25E-10	6	18	0.527	1.00E-10
7	15	21	0.665	2.85E-12	13	20	0.650	1.00E-13
8	9	15	0.366	1.99E-19	6	17	0.439	1.00E-18
9	7	15	0.302	2.57E-19	5	16	0.384	1.00E-22
10	15	22	0.697	1.25E-11	14	21	0.687	1.00E-12
11	15	19	0.553	4.62E-21	12	20	0.592	1.00E-22
12	9	15	0.366	1.99E-19	6	17	0.439	1.00E-18

Table 1. Comparison Between AMI and Linkeye Before Optimization.

Figure 4 shows the block diagrams of the AMI model and its corresponding LinkEye model, in which the mappings of the S-parameters of the TX driver, TX package, RX load, and RX package from LinkEye to AMI are illustrated. S_AMI_txd and S_AMI_rxl are the on-die S-parameters used in the AMI model.

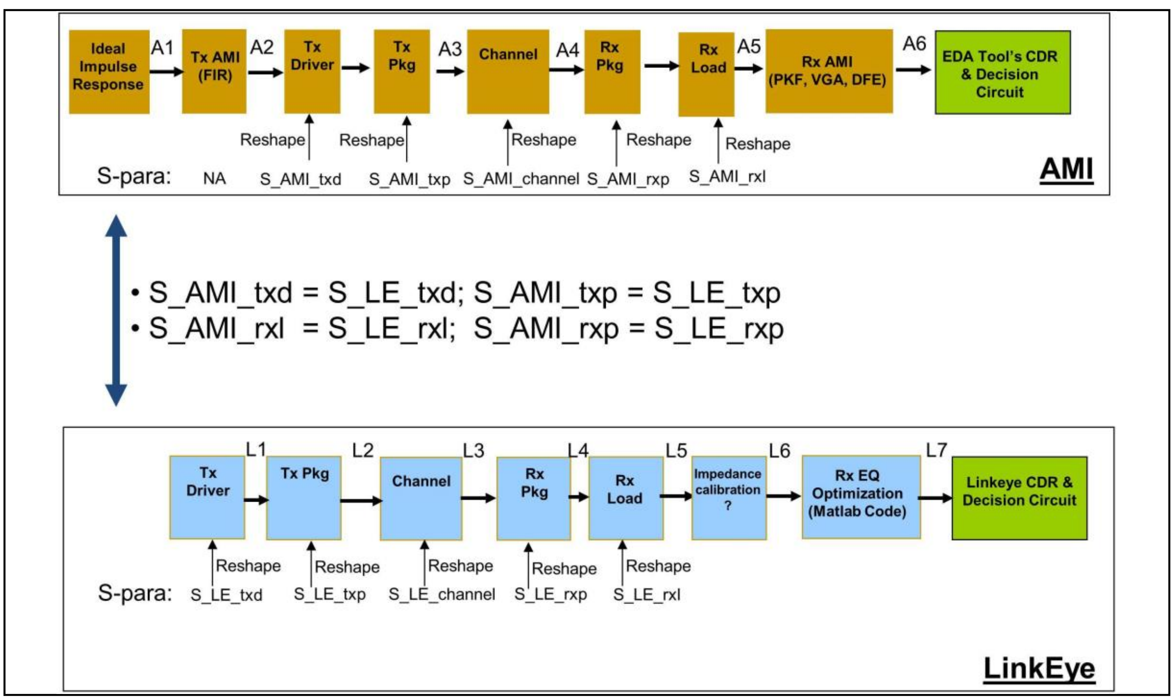


Figure 4. Block Diagrams of 11.5G IBIS-AMI Model and Linkeye Model.

First, we did a sanity check on RX block. In this procedure, the input to AMI RX block (A5) is forced to be the same as that to LinkEye RX block (L6), and both output pulses from AMI RX and LinkEye RX are compared along with some other critical output parameters. As shown in Figure 5, given the same input, the output of AMI RX model shows a good match with that of LinkEye, not only in pulse shapes, but also in EQ parameters, which implies that AMI RX correlated well with LinkEye.

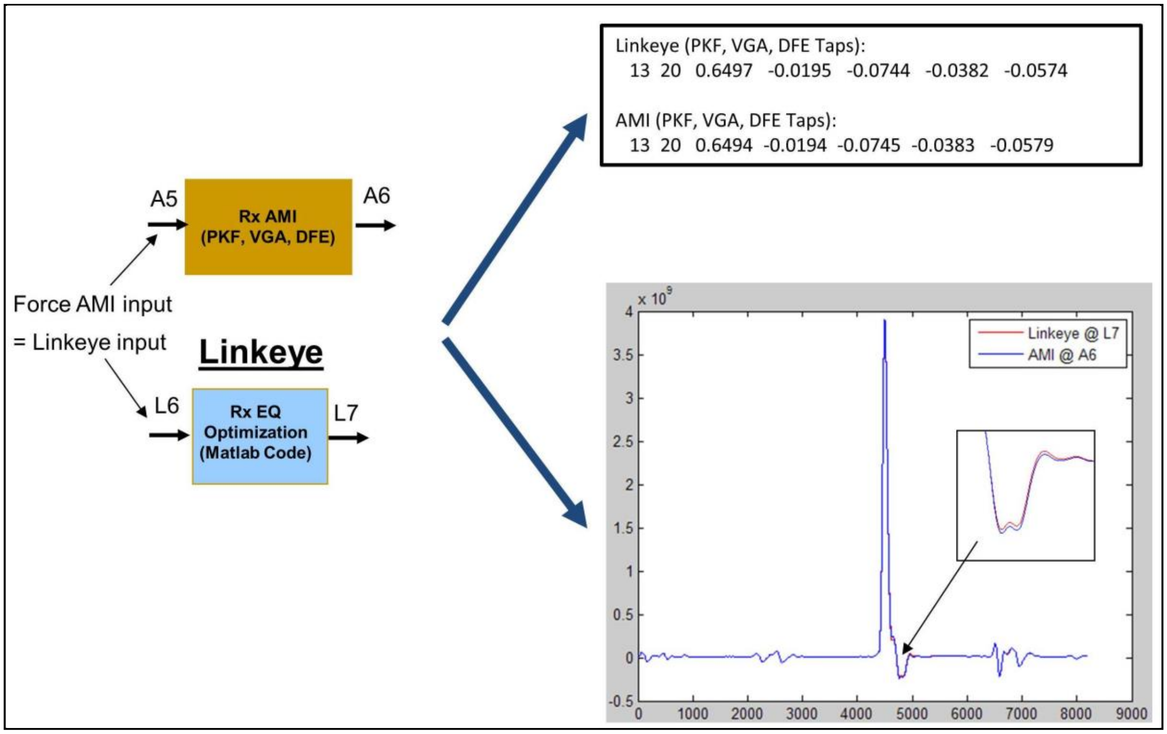


Figure 5. RX Block Sanity Check.

Second, since impulse response (IR) is used in AMI modeling while pulse response (PR) is used in LinkEye, our next step in the optimization procedure is to verify that the IR/ PR conversions in the EDA tool and LinkEye match each other and generate identical results. Figure 6 and Figure 7 show the verification test for IR to PR and PR to IR conversions, respectively, and the exactly matched pulses indicate that the EDA tool has the same operation on the IR/PR conversion as in LinkEye.

Third, the actual inputs to RX blocks of AMI and LinkEye are compared. For the AMI model, the input is given by the inverse Fourier transform of the cascading of S_AMI_txd, S_AMI_txp, S_AMI_channel, S_AMI_rxp and S_AMI_rxl convolved with an “ideal impulse” in the EDA tool as indicated in Figure 4 (top). Here, we use the term of “ideal impulse” instead of Dirac delta function because we don’t know what exactly the EDA tool use but we think it is supposed to be close to Dirac delta function. We can still use this method to debug and correlate our AMI model to LinkEye to certain level. On the other hand, for the LinkEye model, it is simply the inverse Fourier transform of the cascaded S-parameters including S_LE_txd, S_LE_txp, S_LE_channel, S_LE_rxp and S_LE_rxl, as described in Figure 4 (bottom). In our example as shown in Figure 8, we then calculated the pulse response and we saw the EDA tool has introduced some deviation from the LinkEye output (left-hand side). However, the raw pulse shape (as defined in Figure 8) shows a good agreement with the LinkEye pulse. Given the fact that we have validated the entire RX block in step 1 and IR/PR conversion method in step 2, we know there is a format or syntax issue in specifying S_AMI_txd for the EDA tool.

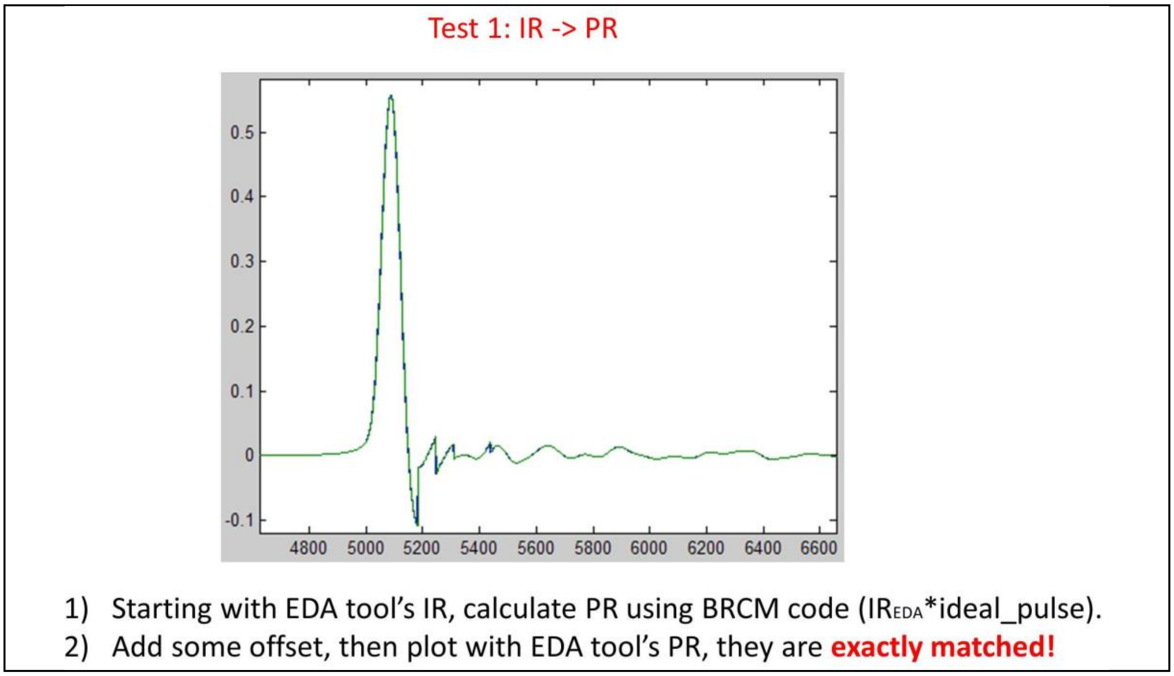


Figure 6. IR to PR Conversion.

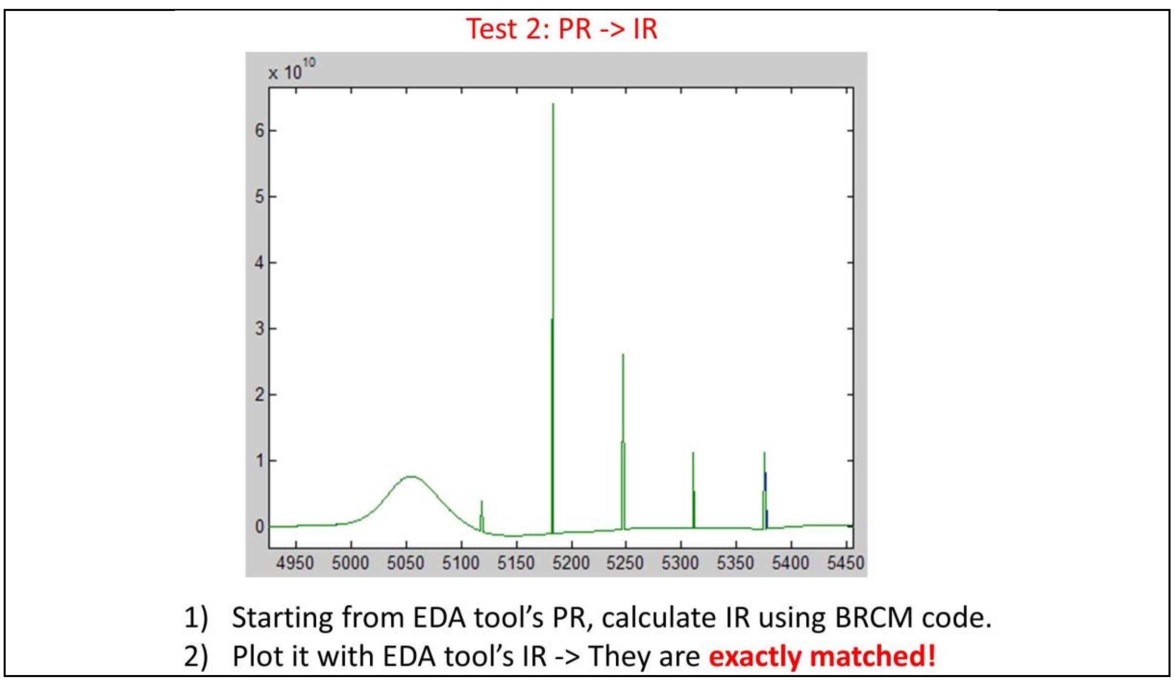


Figure 7. PR to IR conversion.

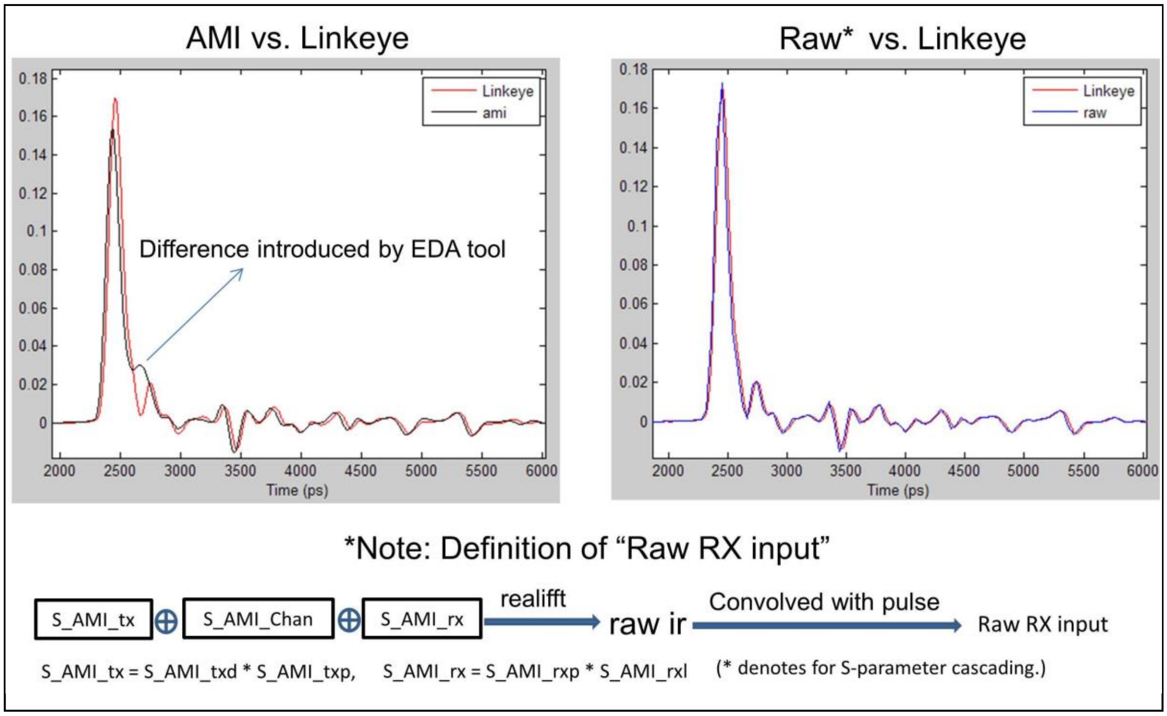


Figure 8. Comparison of RX Block Pulse Inputs Between AMI and Linkeye.

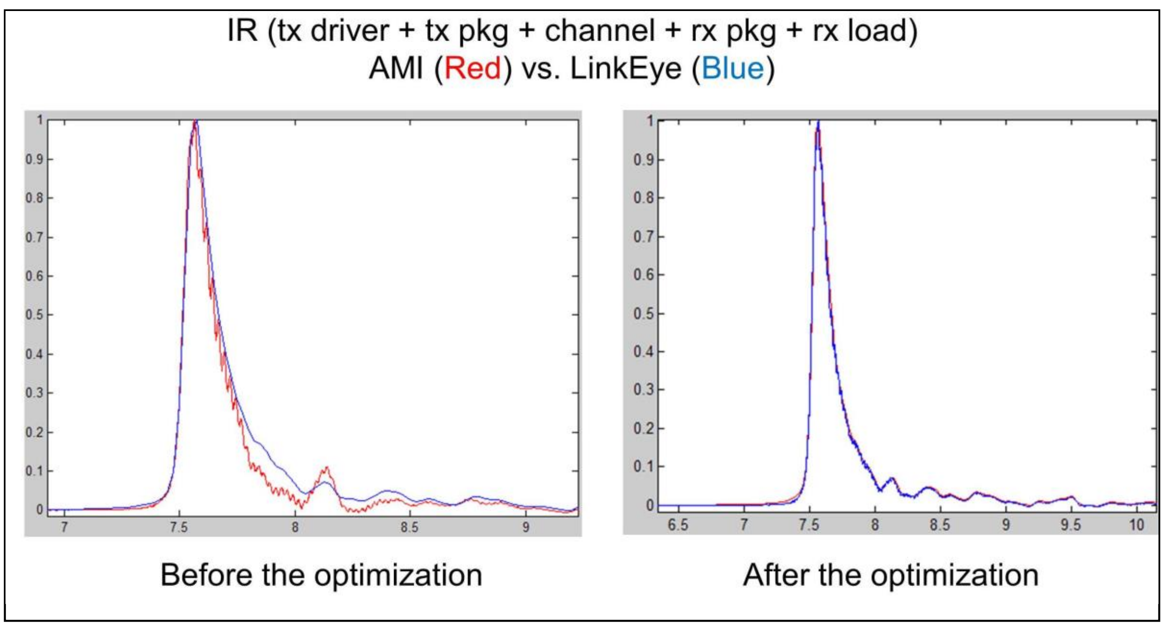
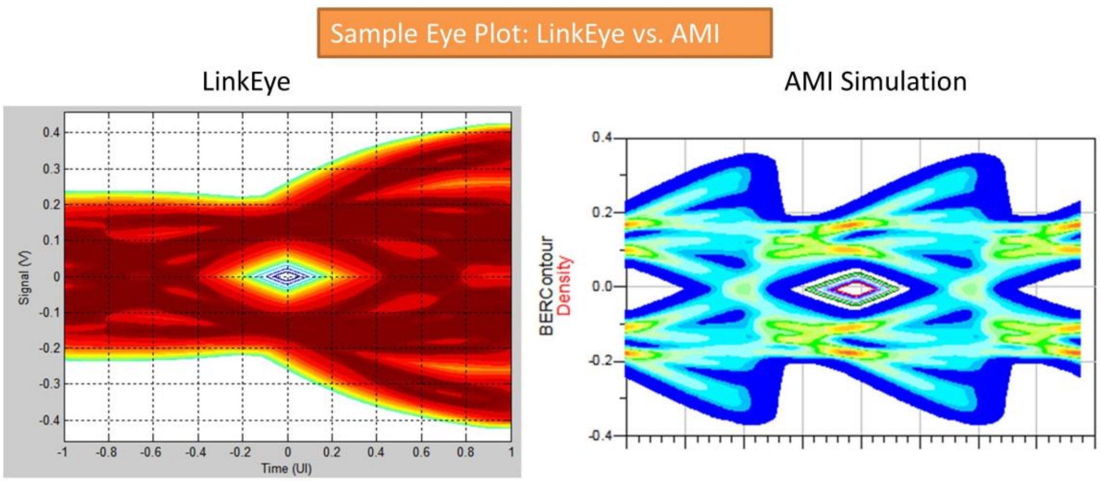


Figure 9. Optimization of On-Die S Parameters in EDA Tools.

After working with the EDA tool vendor, we optimized the TX on-die S parameters (S_AMI_txd) to get better correlation between the AMI model and LinkEye. Figure 9 shows the results before and after on-die S parameters optimization, and it can be seen that the correlation between AMI and LinkEye has improved remarkably after the optimization. Note that the channel used in Figure 9 is different from the one used in Figure 8.



Simulation Results: LinkEye vs. AMI

SimID	Pre-cursor	Main	Post-cursor	LinkEye Simulation Results							AMI Simulation Results						
				PF_Low	PF	VGA	DFE Tap1	DFE Tap2	Eye Width	Eye Height	PF_Low	PF	VGA	DFE Tap1	DFE Tap2	Eye Width	Eye Height
316	0	0.8	0	3	10	11	0.852	0.188	0.23UI	11%	3	9	11	0.859	0.192	0.25UI	12.40%
316	-0.125	0.8	0	3	8	13	0.842	0.193	0.25UI	12.40%	3	8	13	0.847	0.185	0.27UI	14.00%

Figure 10. Simulation Results for AMI Model and Linkeye Model in 11.5G SerDes Case Study.

11.5G LinkEye vs. EDA Tool Correlation (Typ. PVT)

Channel ID	IL @5.75GHz (dB)	Veye (mv)	Heye (ps)	Tx FIR	VGA	PF1	PF2	DFE1
1	7.8	122	38.4	[-0.125 0.675 0.000]	27	1	3	0.541
		107	43.9		27	1	3	0.528
2	12.9	113	38.4	[-0.125 0.675 0.000]	27	4	5	0.644
		93	43.0		28	3	5	0.649
3	14.3	88	30.3	[-0.125 0.675 0.000]	28	5	5	0.669
		90	39.5		29	5	5	0.692
4	15.0	114	38.4	[-0.125 0.675 0.000]	31	3	5	0.710
		119	46.5		31	3	5	0.706
5	16.8	101	34.4	[-0.125 0.675 0.000]	29	6	6	0.717
		79	43.4		29	6	6	0.740
6	17.6	115	38.4	[-0.125 0.675 0.000]	31	5	6	0.750
		112	47.3		32	4	6	0.773

Table 2. Correlation Results of Linkeye and AMI Model for 11.5G SerDes.

Up to now, the AMI model has been optimized to correlate with LinkEye and the simulation results based on certain EDA platforms are compared with LinkEye for the example of 11.5G SerDes in this case study. It can be seen in Figure 10 that both the eye pattern and critical parameters (peaking filter, VGA, and DFE) are closely matched between the AMI model and the LinkEye model.

We ran a few more tests for 11.5G SerDes, and the correlation results of LinkEye (blue) and EDA tools (red) at typical process, voltage, and temperature (PVT) are listed in Table 2. Both TX and RX correlations are considered. It can be seen that the AMI model has a good agreement with the LinkEye simulations in terms of the parameters set of [V-eye, H-eye, VGA, PF1, PF2, DFE].

5. Case Studies: IBIS-AMI Model Validation Through Model-to-Lab Correlation

While direct correlation to LinkEye is straightforward and effective, in many cases we also do model-to-lab correlation especially when the LinkEye code has not been built for some open-eye applications. In this section, a 10G 40nm XFI SerDes and a SFI-5.1 to OTU3 (2x23Gbps D-QPSK) multiplexer are investigated. For 10G 40nm XFI, both the transmitter and receiver AMI models are correlated with measured data in the lab test. For the SFI-5.1to OTU3 (2x23Gbps D-QPSK) MUX, we studied 23G Tx correlation.

5.1 10G 40nm XFI – Transmitter-only Correlation

Figure 11 shows the schematic of the 10G 40nm XFI AMI model used for TX correlation. The BCM84754 is connected as a TX while at the receiver end, an ideal RX termination is used. A measurement setup is illustrated in Figure 6, in which the TX output eye diagram is measured with an Agilent DCA.

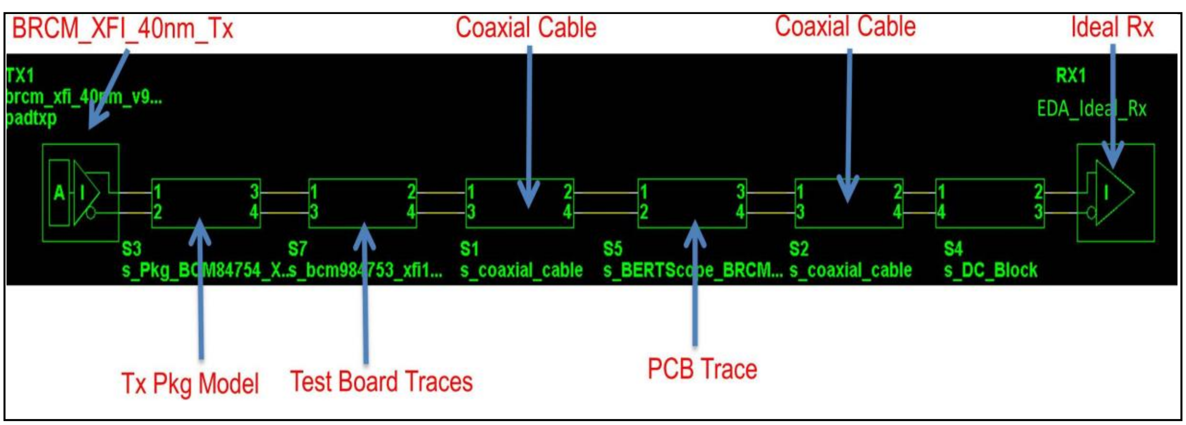


Figure 11. 10G 40nm XFI IBIS-AMI Model for TX Correlation Test.

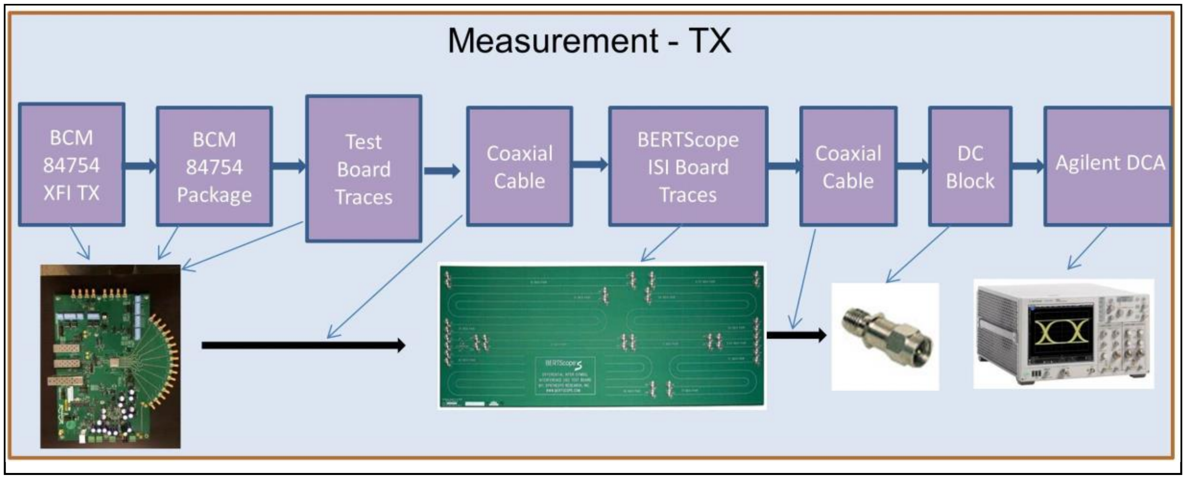


Figure 12. Measurement Setup for TX Correlation.

Two test cases with different sets of trace length, main tap, and post-cursor are investigated for TX correlation. The results are summarized in Table 3 and Table 4 for BER of 1e-6 and 1e-12, respectively. It can be seen that in both cases, the simulation results (Red) shows a good agreement with the measurements (Black).

Test ID	Trace length (inch)	Main tap	Post-cursor	Eye Height (inner) @1e-6 (mv)		Eye Height (outer) @1e-6 (mv)		Eye Width (inner) @1e-6 (ps)	
				Measured	Simulation	Measured	Simulation	Measured	Simulation
Case 1	12	21	8	177	169	359	381	77	73
Case 2	31	17	14	85	79	229	229	69	70

Table 3. 10G 40nm XFI TX Correlation at BER of 1e-6.

Test ID	Trace length (inch)	Main tap	Post-cursor	Eye Height (inner) @1e-12 (mv)		Eye Height (outer) @1e-12 (mv)		Eye Width (inner) @1e-12 (ps)	
				Measured	Simulation	Measured	Simulation	Measured	Simulation
Case 1	12	21	8	148	146	388	399	65	64
Case 2	31	17	14	69	69	250	240	60	63

Table 4. 10G 40nm XFI TX Correlation at BER of 1e-12.

Eye patterns for test case 1 and 2 at BER of 1e-6 and 1e-12 are shown in Figure 13 and Figure 14. Both cases shows a good match between the eye measurements and calculations for the Tx correlation test..

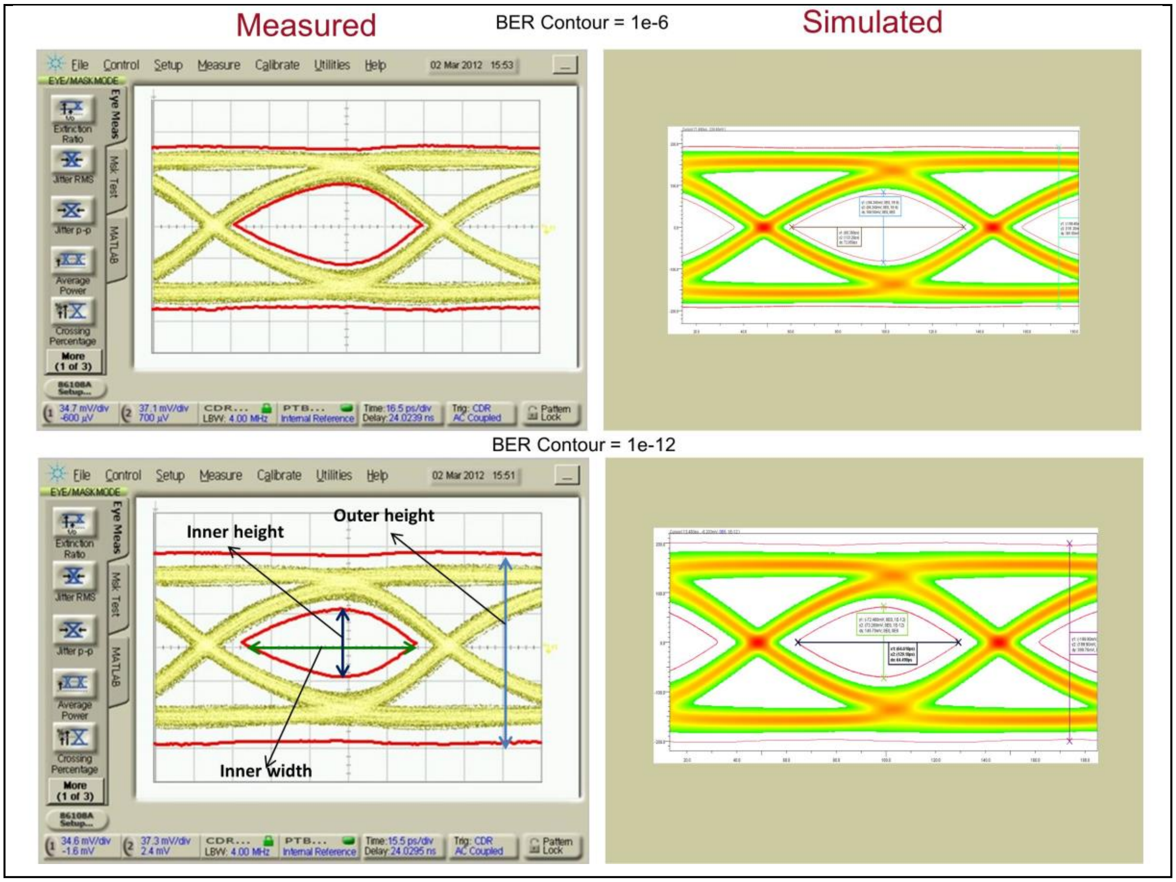


Figure 13. 10G 40nm XFI TX Correlation Test Case 1 with Trace =12”, Main_tap = 21 and Post-Cursor = 8.

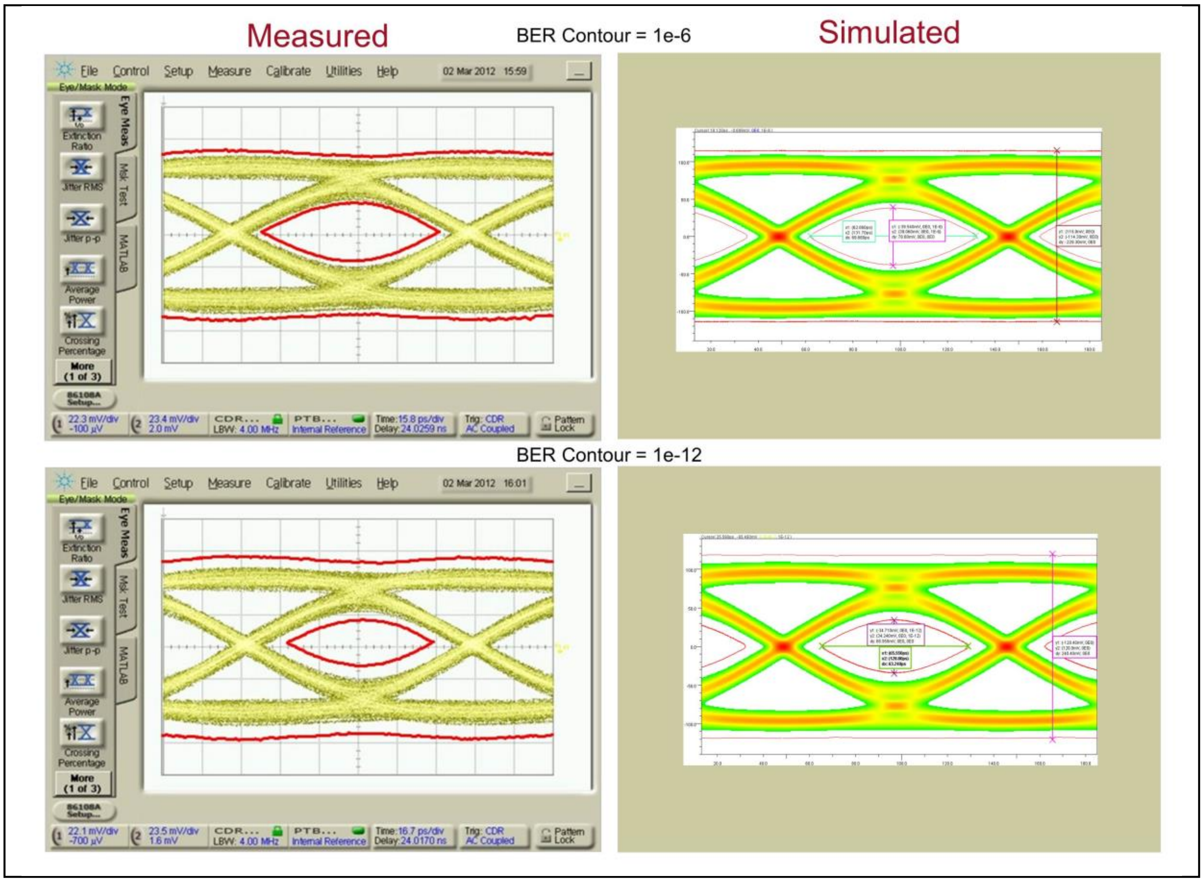


Figure 14. 10G 40nm XFI TX Correlation Test Case 2 with Trace =31", Main_tap = 17 and Post-Cursor = 14.

5.2 10G 40nm XFI – Transmitter and Receiver Correlation

In this step, the ideal receiver is replaced with Broadcom's 10G 40nm XFI receiver and the correlation test is repeated. The corresponding schematics of the IBIS-AMI model and measurement setup are shown in Figure 15 and Figure 16, respectively.

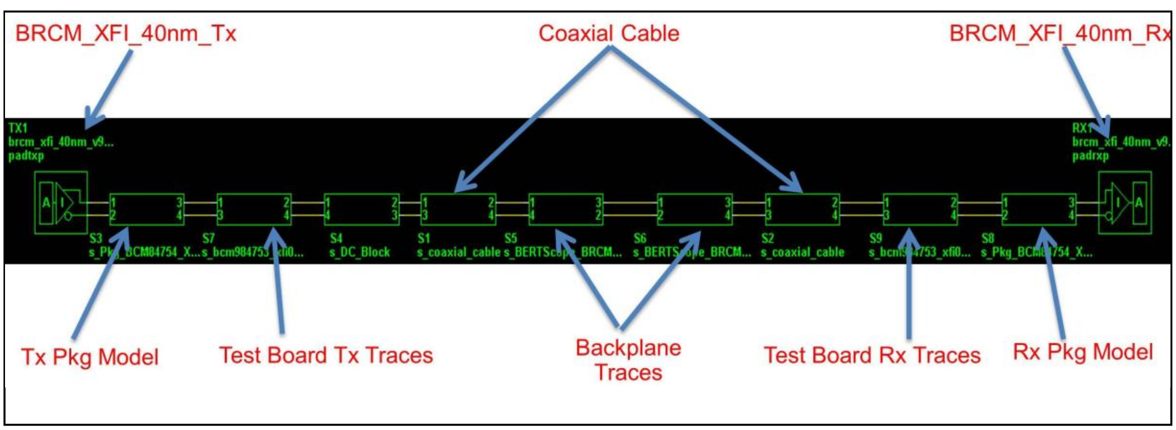


Figure 15. 10G 40nm XFI IBIS-AMI Model for TX+RX Correlation Test.

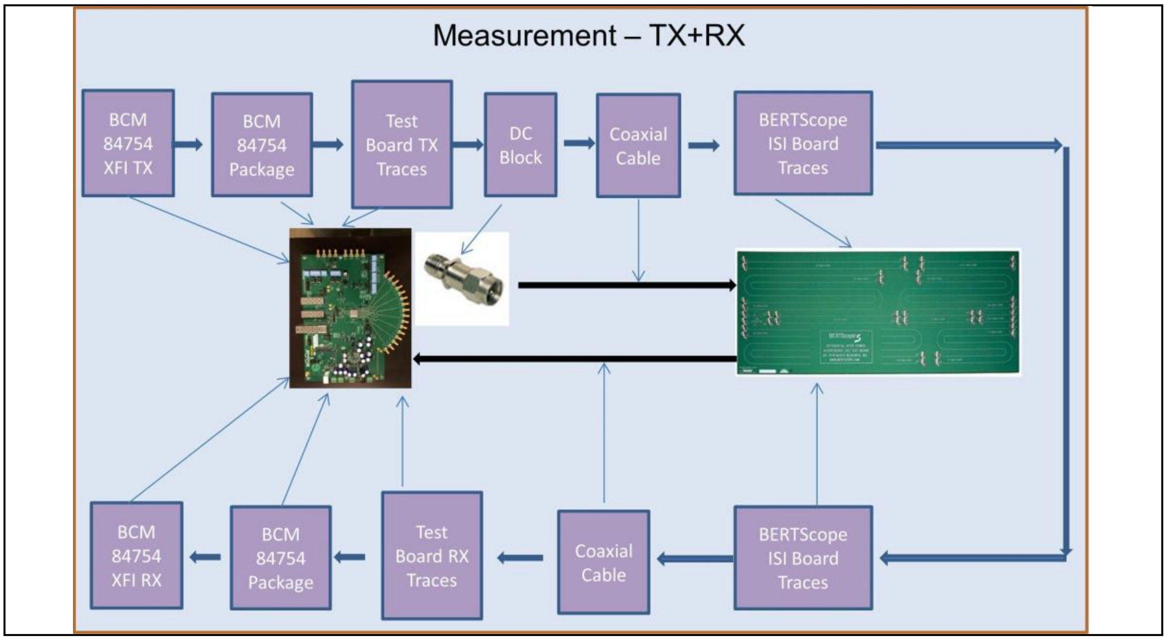


Figure 16. Measurement Setup for TX+RX Correlation Test. BER measurement is inside the Rx using the BIST (built-in Self-Test) feature of the chip

Test results for lab measurements and simulation calculations are listed in Table 5.

Test ID	Trace (inch)	Tx Main Tap	Tx Post Tap	Rx Peaking Filter	Measured BER	Simulated BER
Case 1	31+12	24	0	14	3.0E-7	7.5E-5
Case 2	31+24	24	15	8	3.4E-12	1.8E-11
Case 3	31+12	24	0	8	<1E-14 (no errors in 2 hrs)	1.5E-32
Case 4	31+5	24	10	4	<1E-14 (no errors in 2 hrs)	2.8E-86

Table 5. 10G 40nm XFI TX+RX Correlation Results.

It can be seen from Table 5 that in high-BER cases (cases 1 and 2), measured BER is slightly better than simulated BER. In low-BER cases (cases 3 and 4), no error is captured for both measurements and simulations. Again the results show there is a good match between 10G 40nm XFI AMI models and the lab measurements.

5.3 SFI-5.1 to OTU3 (2x23Gbps D-QPSK) MUX Transmitter Correlation #1: TX Output

In this case study, a SFI-5.1 to OTU3 (2x23Gbps D-QPSK) MUX Transmitter is used for a model-to-lab correlation test. In this study, a HS MMPX-SMA cable is used for the connection between TX and RX and an ideal receiver is selected for the TX correlation test. The simulation model in an EDA tool is given in Figure 17.

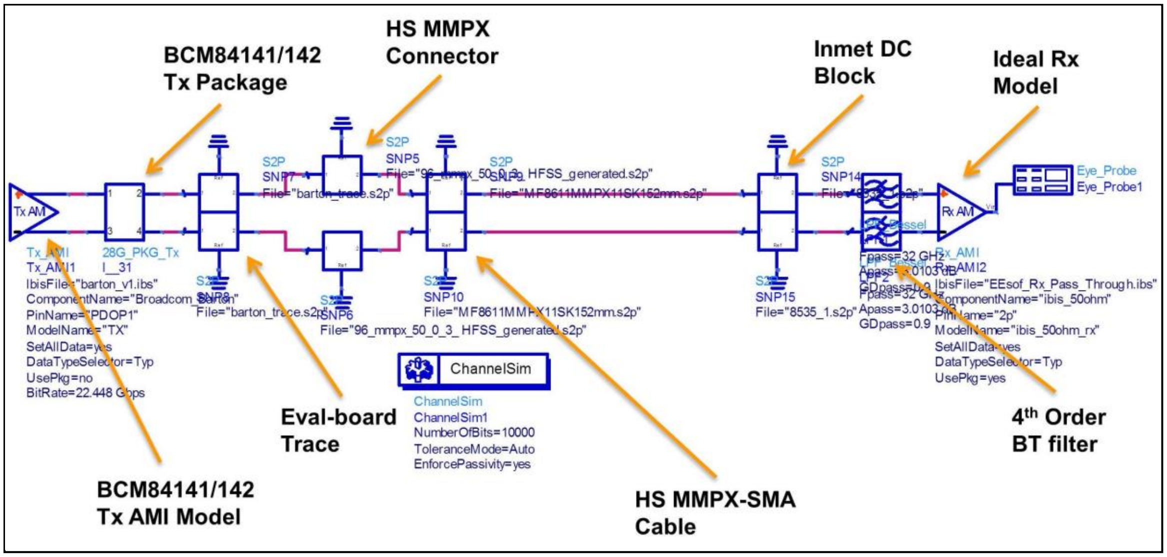
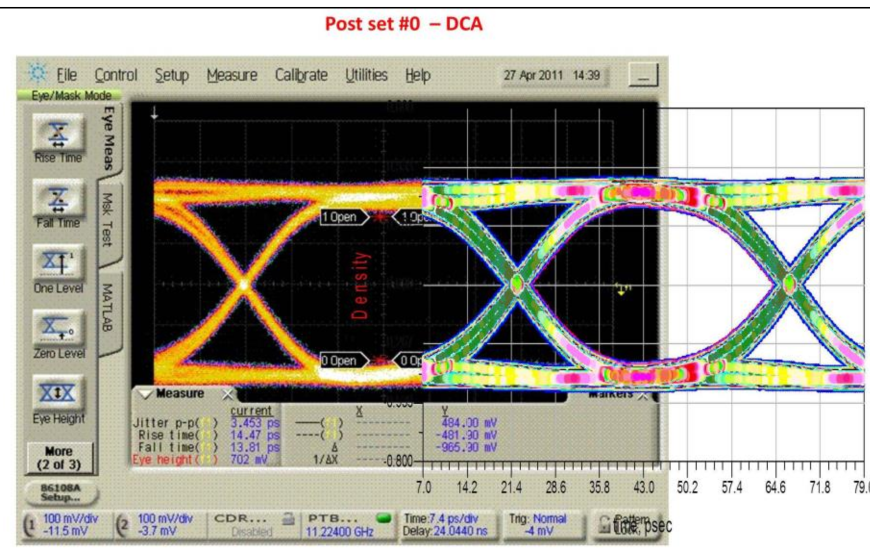


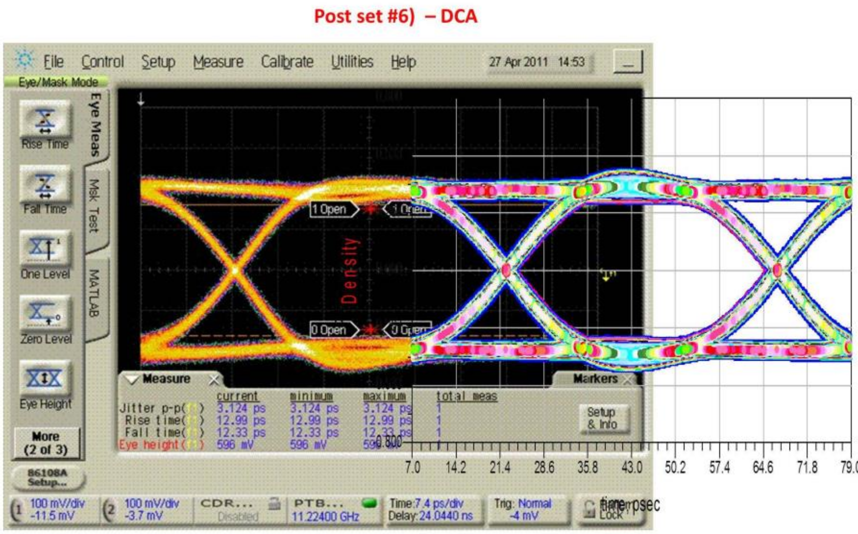
Figure 17. BCM84141/142 AMI Simulation Model.

Six test cases are studied with different preemphasis settings. The eye diagrams are plotted in the EDA tool and compared with captured eye patterns from Agilent DCA. In test cases with post-cursor settings of 0, 6, and 12, TX jitter, rise time, fall time, and eye height are also measured (lab testing) and calculated (AMI).



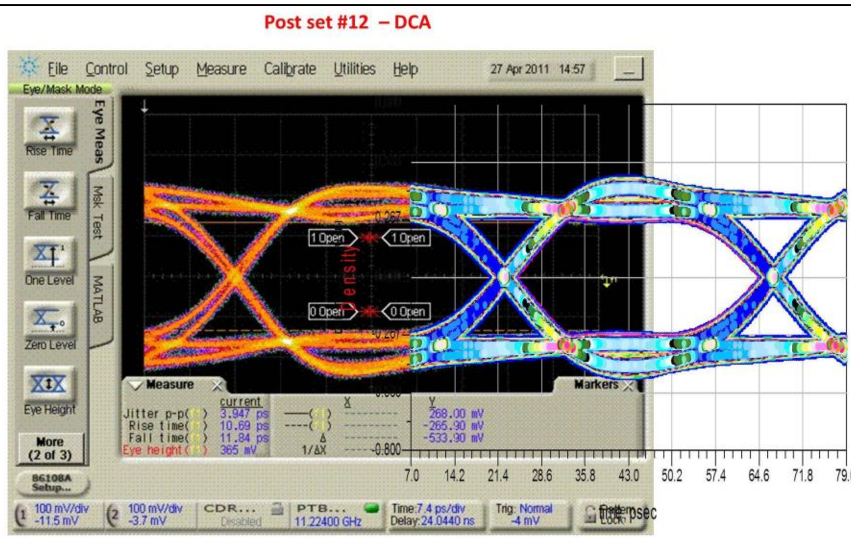
	Jitter_pp (ps)	Rise time (ps)	Fall time (ps)	Eye Height (mV)
Simulated	3.02	14.86	14.79	709
Measured	3.45	14.47	13.81	702

Figure 18. Measured and Simulated Eye Patterns and Parameters for Post-Cursor Setting of 0.



	Jitter_pp (ps)	Rise time (ps)	Fall time (ps)	Eye Height (mV)
Simulated	1.78	14.07	14.02	634
Measured	3.12	12.99	12.33	596

Figure 19. Measured and Simulated Eye Patterns and Parameters for Post-Cursor Setting of 6.



	Jitter_pp (ps)	Rise time (ps)	Fall time (ps)	Eye Height (mV)
Simulated	2.68	13.74	13.68	522
Measured	3.95	10.69	11.84	534

Figure 20. Measured and Simulated Eye Patterns and Parameters for Post-Cursor setting of 12.

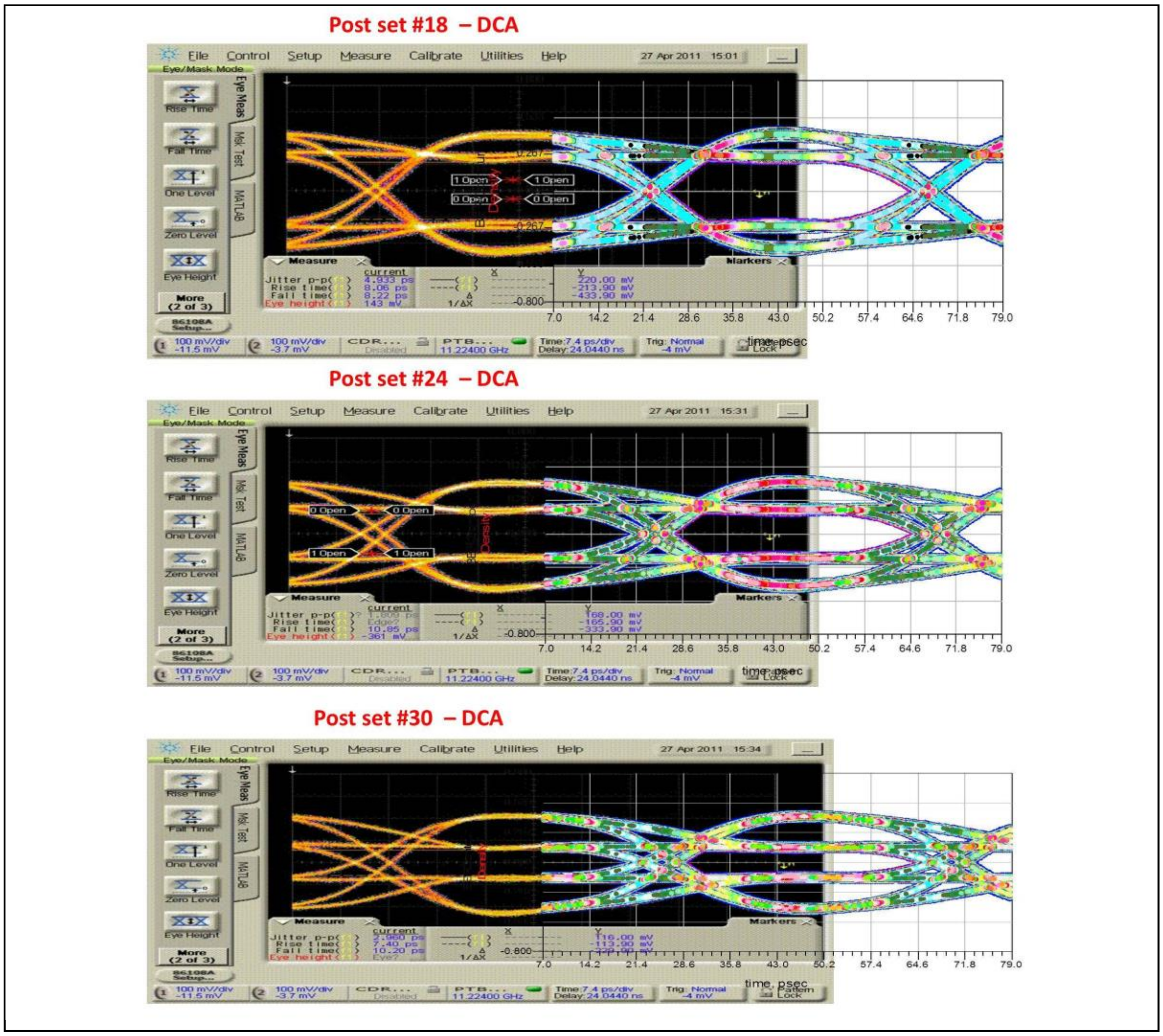


Figure 21. Measured and Simulated Eye Patterns for Post-Cursor Setting of 18, 24 and 30.

Figure 18 through Figure 20 shows the results for the post-cursor set # of 0, 6, and 12, with the measured/calculated parameters. Figure 21 shows the results for the post-cursor set # of 18, 24, and 30.

5.4 SFI-5.1 to OTU3 (2x23Gbps D-QPSK) MUX Transmitter Correlation #2: TX with 6" FR4

In this case study, we added a 6" FR4 trace between the Tx and the ideal Rx. All other setups are kept the same.

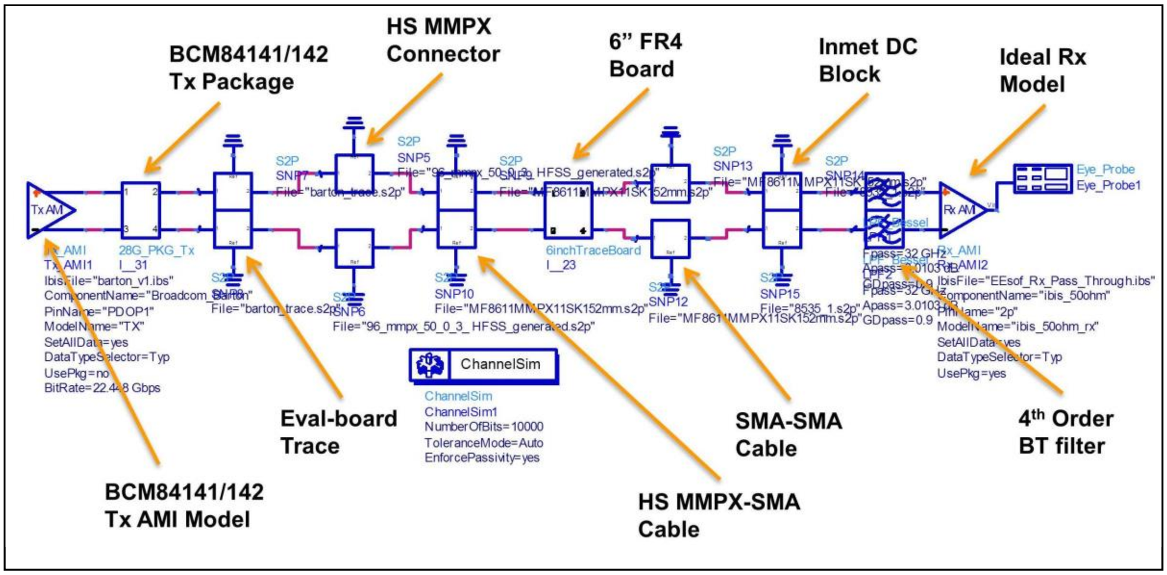
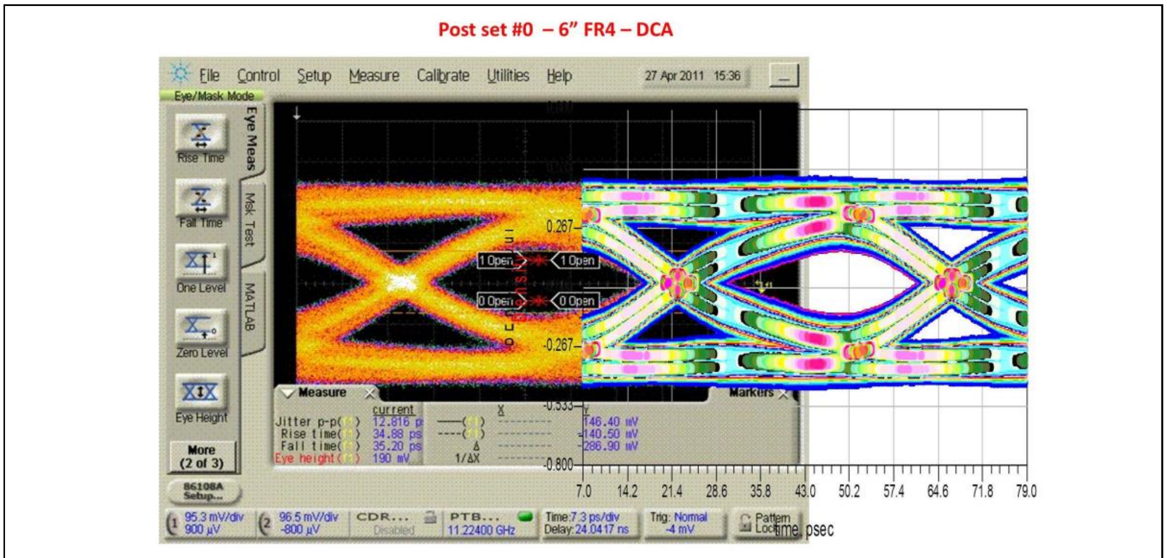


Figure 22. BCM84141/142 AMI Simulation Model with FR4.

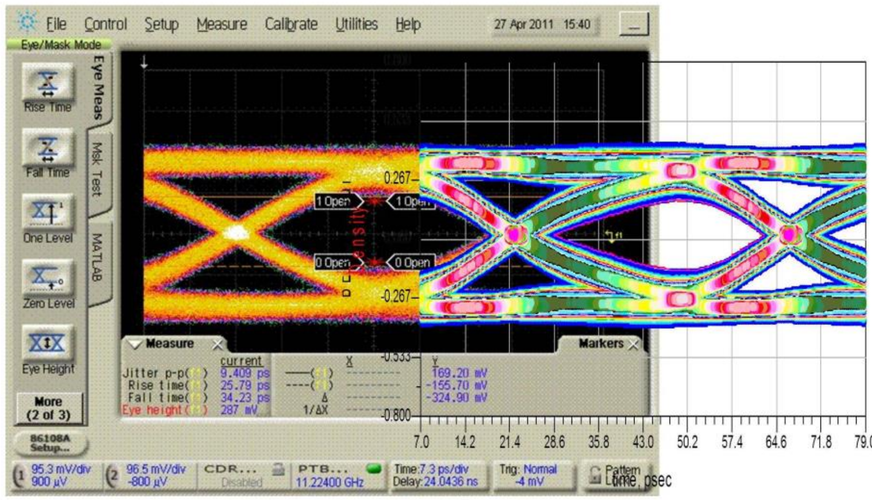
The TX correlation test is repeated and the results for test cases with the post-cursor set # of 0, 6, 12, 18, 24, and 30 are shown along with eye patterns of the measured and calculated parameters (for set # of 0, 6, 12, and 18).



	Jitter_pp (ps)	Rise time (ps)	Fall time (ps)	Eye Height (mV)
Simulated	9.84	24.28	24.07	229
Measured	12.82	34.88	35.20	287

Figure 23. Measured and Simulated Eye Patterns and Parameters for Post-Cursor Setting of 0 with 6" FR4.

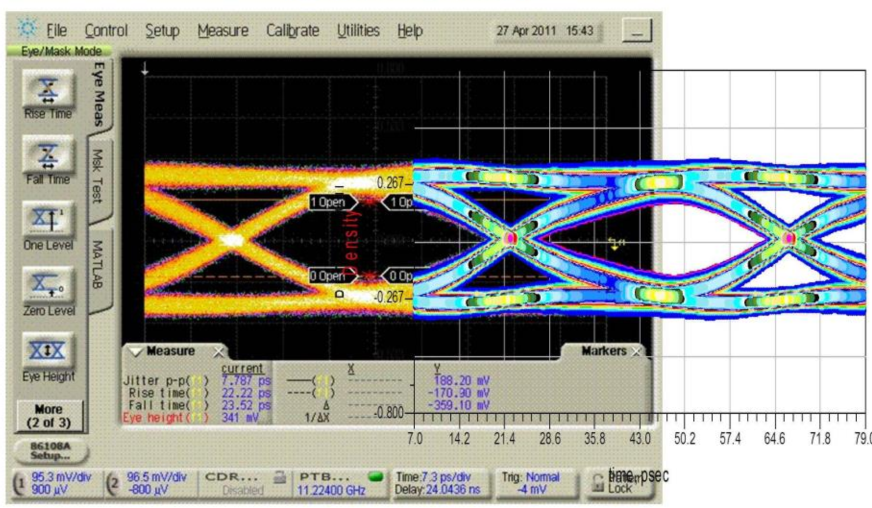
Post set #6 – 6" FR4 – DCA



	Jitter_pp (ps)	Rise time (ps)	Fall time (ps)	Eye Height (mV)
Simulated	6.07	21.60	21.74	303
Measured	9.41	25.79	34.23	325

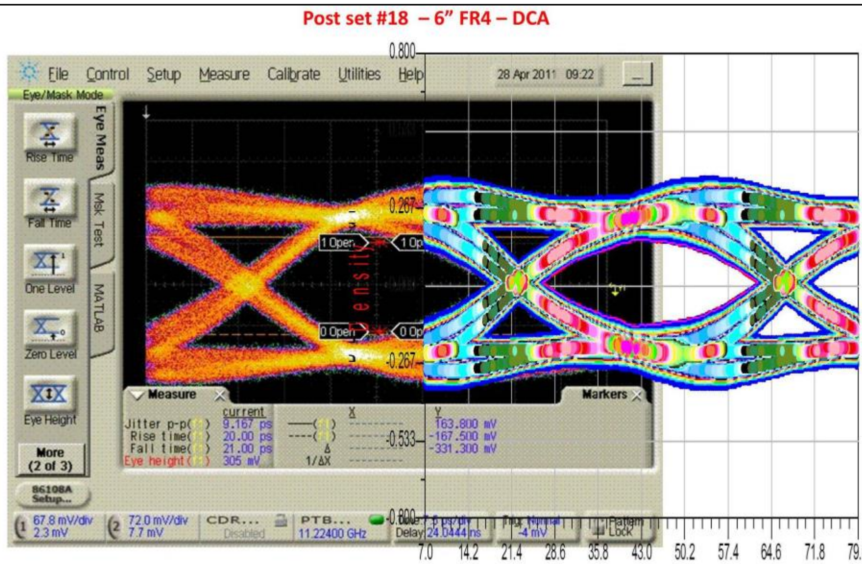
Figure 24. Measured and Simulated Eye Patterns and Parameters for Post-Cursor Setting of 6 with 6" FR4.

Post set #12 – 6" FR4 – DCA



	Jitter_pp (ps)	Rise time (ps)	Fall time (ps)	Eye Height (mV)
Simulated	3.46	19.67	20.08	355
Measured	7.79	22.22	23.52	359

Figure 25. Measured and Simulated Eye Patterns and Parameters for Post-Cursor Setting of 12 with 6" FR4.



	Jitter_pp (ps)	Rise time (ps)	Fall time (ps)	Eye Height (mV)
Simulated	5.69	18.35	18.87	324
Measured	9.17	20.00	21.00	331

Figure 26. Measured and Simulated Eye Patterns and Parameters for Post-Cursor Setting of 18 with 6" FR4.

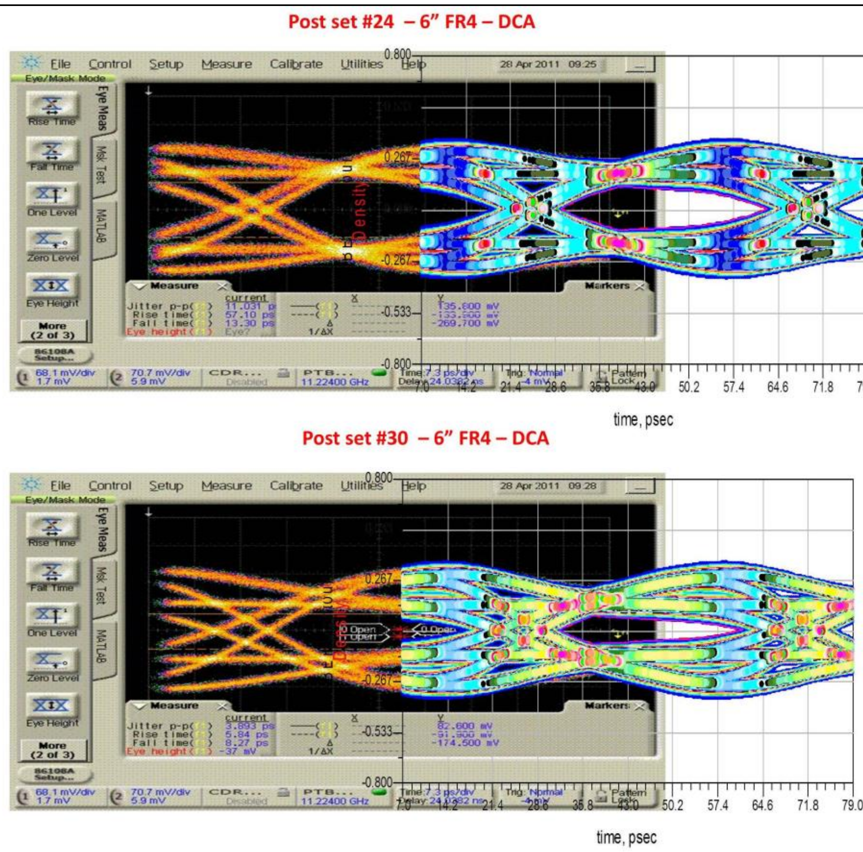


Figure 27. Measured and Simulated Eye Patterns for Post-Cursor Setting of 24 and 30 with 6" FR4.

For TX correlation of BCM84141/142 with 6" FR4+DCA, eye patterns and corresponding measured/calculated parameters are shown in Figure 23 through Figure 26 for post-cursor set # of 0, 6, 12, and 18. For post-cursor set # of 24 and 30, only eye diagrams from measurements and simulations are compared, as shown in Figure 27. Considering all of the above results, we can conclude that the SFI-5.1 to OTU3 (2x23Gbps D-QPSK) MUX Transmitter AMI model correlates well with the lab measurements, despite some small eye parameters deviation.

6. Discussion: How to Choose a Proper IBIS-AMI Model Validation Method

In the above case studies, we have presented basic procedures for two IBIS-AMI model validation methods: model-to-model and model-to-lab correlation. Although either of these methods can be used to validate AMI models, there are significant differences, and one should choose a proper validation method based on specific conditions and requirements. Model-to-lab correlation provides the ultimate benchmark for the validation of an AMI model because all the measurements result comes from the real chips and links. However, test bench setup can be difficult and time-consuming and taking component and measurement variation into account can be extremely difficult. When an in-house simulation model like LinkEye tool is available and proved to correlate well with real chip measurements, model to model correlation method is preferred. In our case, correlating with LinkEye models provided a more flexible choice in AMI model validation for most closed-eye applications where complicated equalization schemes are used. However, if a previous model is not available or significant hardware or DSP algorithm changes have been implemented in a new chip design, the model-to-lab correlation method will be the only available option.

7. Conclusions

In this work, two methods of validating an IBIS-AMI model have been presented. In a 11.5G SerDes case, the model-to-model correlation method is demonstrated in different blocks of the entire data path. For a 10G TX and RX XFI model and a 23G TX model, the model-to-lab correlation method is demonstrated. Both of these methods can provide effective validation results and one should select the proper method based on the availability and completeness of previously developed simulation models as well as the complexities associated with deploying each method.

8. References

[1] IBIS Committee, "IBIS (I/O Buffer Information Specification), version 5.0," August 2008.

[2] Walter Katz, MikeSteinberger and Todd Westerhoff, "IBIS-AMI Terminology Overview," SiSoft, July 2009.

[3] Colin Warwick, Fangyi Rao, "Explore the SerDes Design Space Using the IBIS AMI Channel Simulation Flow," Agilent, 2012.

[4] LinkEye® is a registered trademark of Broadcom Corporation.

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